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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/040,395
Filing Date: January 07, 2002
Appellant(s): YUE ET AL.

Trevor B. Joike
For Appellant

REVISED EXAMINER'S ANSWER

This is in response to Appeal Brief filed on June 02, 2005 in view of Board's *Order Retuning Undocketed Appeal To Examiner* dated December 05, 2005.

Examiner's Note for this revised Examiner's Answer

This revised examiner's answer, which vacates the previous examiner's answer dated August 2, 2005, addresses the concerns raised in Board's *Order Retuning Undocketed Appeal To Examiner* dated December 05, 2005.

The only difference between this revised examiner's answer and the previous examiner's answer dated August 2, 2005 resides in Section 5 (Summary of the Claimed Subject Matter), in order to comply with the new rules which became effective on September 13, 2004.

This new Section 5 now reads:

(5) Summary of the Claimed Subject Matter

The summary of claimed subject matter contained in the brief is basically correct.

Other sections are unchanged with respect to the previous examiner's answer dated August 2, 2005.

In addition, it is noted that the appellants have been notified in a separate office action the examiner's decision regarding the issue of the IDS filed on May 16, 2003, which was also raised in the Board's *Order Retuning Undocketed Appeal To Examiner* dated December 05, 2005.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The brief does not contain a statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief. Therefore, it is presumed that there are none. The Board, however, may exercise its discretion to require an explicit statement as to the existence of any related appeals and interferences.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is basically correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

The following is a listing of the evidence (e.g., patents, publications, Official Notice, and admitted prior art) relied upon in the rejection of claims under appeal.

5,038,184	Chiang et al.	06 August 1991
6,100,770	Litwin et al.	08 August 2000
5,563,438	Tsang	08 October 1996

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 32-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al. ("Chiang"; US 5,038,184) in view of Litwin et al. ("Litwin"; US 6,100,770).

Chiang discloses a method for making a varactor (see Figs. 2-3 and 7, especially Fig. 7; also see col. 4, lines 26-36, col. 5, lines 7-64, and col. 7, lines 32-35), comprising: forming a plurality of alternating lightly doped wells or body regions (47; col. 5, lines 7-10) and heavily doped N+ region regions (45a through 45n; col. 5, lines 61-64) in a silicon layer of an SOI structure; forming a plurality of gate oxides (44); forming a plurality of polysilicon gates (46); electrically coupling each of the polysilicon gates together; and, electrically coupling each of the heavily doped second conductivity type region regions together, wherein the lightly doped wells or body regions (47) and the heavily doped N+ regions (45a—45n) all extend from the top to the bottom of semiconductor layer (42).

Although Chiang does not expressly disclose that each of the lightly doped wells or body regions can be P-type doped, one of ordinary skill in the art would readily recognize that the lightly doped well or body region in an varactor can each be commonly and desirably P-type lightly doped for forming a depletion-type channel region with good channel modulation sensitivity (i.e., an NMOS-enhancement-transistor-like varactor), as evidenced in Litwin (see the P-type lightly doped well or body region (22) and the heavily doped N+ region in the varactor of Fig. 2; also see col. 4, lines 8-29).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the making of the P-type lightly doped well

or body region of Litwin into the method of Chiang, so that a method for making a varactor with a commonly desired highly sensitive depletion-type channel regions would be obtained. And, with the P-type lightly doped wells or body regions being formed in the above collectively taught method, N+/P- junctions would be naturally formed therein.

Regarding claims 34-36, it is art-known that silicon-insulator substrates of both the silicon-on-oxide type (SOI type, which normally naturally includes a highly resistive silicon bottom layer) and the silicon-on-sapphire type (SOS) had become readily available for either N-channel or P-channel type MOS devices, as readily evidenced in the prior art such as Tsang (US 5,563,438; see col. 3, lines 36-37).

Regarding claim 37, with the P-type lightly doped wells or body regions being formed in the above collectively taught method, N+/P- junctions would be naturally formed therein, which in turn would cause the P-type wells or body regions to be inherently floated electrically, due to the electrical isolation naturally provided by the N+/P- junctions.

Regarding claim 38, Litwin further teaches that each of the silicon gates can have a width-to-length ratio in a range covering a ratio of approximately 16 to 1 (see col.6, lines 10-17).

Regarding claims 39 and 40, with the width-to-length ratio being approximately 16 to 1 in the above collectively taught varactor, which is substantially the same ratio as that in the instant invention, the same width-to-length ratio should result in a substantially same effect (if there is one) on the above collectively taught varactor. Thus, the capacitor switching ratio in the collectively taught varactor should be

substantially similar to the one of the instant invention, provided that the gate-ground ratio is approximately optimized, as already recognized in Chiang (col. 6 and 7). And, the gate width, gate length, and gate-ground overlap are art-recognized result-effective importance parameters for the capacitive switching ratio, and they all are subject to routine experimentation and optimization.

Response to Arguments

Applicant's arguments filed in the 02-10-2005 Brief have been fully considered but they are not persuasive, as explained in details below.

Response to Arguments of ISSUE 1 (Pages 9-18 in the Brief)

Appellant argues against the above obviousness rejections by raising the first through fourth alleged problems (pages 11-18 in the Brief). However, these arguments are not persuasive either individually or collectively.

As shown in the above obviousness rejections, Chiang discloses the claimed invention of a method for making a varactor (Fig. 7, also see Figs. 2 and 3 for explanations about the relevant elements therein), including the steps of forming a plurality of alternating lightly doped wells or body regions (47; col. 5, lines 7-10) and heavily doped N+ region regions (45a through 45n; col. 5, lines 61-64) in a silicon layer of an SOI structure, except that Chiang does not expressly disclose that the lightly doped wells or body regions (47) can be P-type doped.

However, Chiang itself already fairly suggests the claimed invention, especially the one defined in claims 32-37 of the instant application, because Chiang teaches that the wells or body regions (47) are lightly doped, given the fact that the conductivity type (thus the doping type) of any doped semiconductor region (including such light doped wells or body regions) has to be one chosen from the only two possible conductivity types (either N-type or P-type), as there is no any other conductivity type existing inside a semiconductor. It is also because there is no any teaching found in Chiang that is against the choosing of the P-type conductivity for the lightly doped wells or body regions (47). And, with the lightly doped wells or body regions (47) being P-type, the resulting method for forming the varactor in Fig. 7 of Chiang should naturally resulting in the formation of each of the features recited in claim 1 of instant application, including the recited N+/P- junctions which naturally exist between any pair of a heavily doped N-type region and a lightly doped P-type region.

Even so, Litwin is still cited by the examiner to show that it is indeed art-known that a lightly doped well or body regions in a varactor can be commonly and desirably doped as P-type when the source/drain regions being N-type doped heavily (see the P-type lightly doped well or body region 22 and the heavily doped N+ source/drain regions 23 and 24 in the varactor of Fig. 2; also see col. 4, lines 8-29), as the one of ordinary skill in the art would readily recognize that the resulting NMOS-enhancement-transistor-like varactor possesses a favorable depletion-type channel region with good channel modulation sensitivity, which inherently result in desirably good capacitance modulation sensitivity.

Accordingly, it would be well within the ordinary skill in the art at the time the invention was made to combine the teachings of Chiang and Litwin, or more specifically to incorporate the making of the P-type lightly doped well or body region of Litwin into the method of Chiang, so that a method for making a varactor with a commonly desired highly sensitive depletion-type channel regions would be obtained. And, such collectively taught method would naturally result in the instant invention as defined in the above rejected claims.

The followings are more specific explanations responding to appellant's alleged first through fourth problems, respectively:

Regarding the alleged first problem (page 11 in the Brief): In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the obviousness rejections as set forth in the final rejection (see the last paragraph on page 4 of the 12-05-2004 final rejection) specifically explains the desirability and/or motivation to one of the ordinary skill about the combination of the teachings of Chiang and Litwin by stating that: "one of ordinary skill in the art would readily recognize that the lightly doped wells or body

regions in an varactor can be commonly and desirably P-type lightly doped for forming a depletion-type channel region with good channel modulation sensitivity (i.e., an NMOS-enhancement-transistor-like varactor), as evidenced in Litwin (see the P-type lightly doped well or body region (22) and the heavily doped N+ region in the varactor of Fig. 2; also see col. 4, lines 8-29)." Such good channel modulation sensitivity is critical to and directly responsible for the main attractive characteristic of the transistor-like varactor—its highly variable capacitance controllable with a voltage applied between the gate electrode and the source/drain electrode. And, appellant's arguments lacks any adequate explanation as to why the above desirability and/or motivation as provided in final rejection is not a valid one. In fact, the appellant is silent about the validity of the provided desirability and/or motivation, which should be regarded as a positive admission to the validity of the provided desirability and/or motivation.

Regarding the alleged second problem (pages 11 and 12 in the Brief): both Chiang (col. 5, lines 7-10) and Litwin (col. 5, lines 36-40) expressly and consistently teach to keep the channel region as a lightly doped region. In fact both of them want the well or body region to be a very lightly doped region. Chiang teaches to form the well or body region (47) from a "very lightly doped" silicon thin film (42) with the formation of the heavily doped source/drain regions (45a through 45n). And, although the well or body region (22) in Fig. 2 of Litwin is marked as "p", it is a commonly acceptable practice in the art to mark a P-type doped region with such a symbol, whether it is lightly doped, or moderately doped, or net doped. One of ordinary skill in the art would readily recognize

that it does not by any means constitute a teaching that the well or body region (22) in Litwin is not a lightly doped region, but a "moderately doped region", as it in the figure only simply shows that the conductivity type of the well or body region (22) therein is p type and it has a doping concentration relatively low compared to the heavily doped source/drain regions (33 and 34; n+). Litwin further clarifies it that the well or body region (22) is a lightly doped region, as Litwin specifically teaches to maintain the well or body region as lightly doped as possible in order to obtain a high dynamic range for the varactor (col.5, lines 36-40).

Furthermore, Appellant argues that Litwin does not teach the features of alternating p- wells and the n+ regions, that Chiang does not teach the lightly doped well or body region is p-type doped, and that neither Chiang nor Litwin teaches the claimed invention. In response to these arguments against the references individually, it is noted that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In this case, Chiang discloses the claimed invention, including the steps of forming a plurality of alternating lightly doped wells or body regions (47; col. 5, lines 7-10) and heavily doped N+ region regions (45a through 45n; col. 5, lines 61-64) in a silicon layer of an SOI structure, except that Chiang does not expressly disclose that P type can be chosen for the lightly doped wells or body regions (47) from the only two possible doping types (P or N). One of ordinary skill in the art would readily recognize that the varactor of Chiang is formed of a plurality of parallel-connected individual

transistor-like varactors each having its own lightly doped well or body region. And, Litwin is cited by the examiner to show that it is indeed art-known that the lightly doped well or body region in such an individual transistor-like varactor can be commonly and desirably doped as P-type when the source/drain regions being N-type doped, in order to form a depletion-type channel region with desirably good channel modulation sensitivity. And, with the P-type lightly doped well or body region in each of the individual transistor-like varactors in the above collectively taught method, N+/P- junctions would be naturally formed between the p-type lightly doped wells or body regions and the heavily doped source/drain regions therein.

Regarding the alleged third problem (pages 12 and 13 in the Brief): In response to these arguments against the references individually, it is noted again that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In this case, Chiang discloses the claimed invention, including the steps of forming the heavily doped N+ region regions (45a through 45n; col. 5, lines 61-64) in a silicon layer (42) overlying a dielectric layer 43 in an SOI structure, except that Chiang does not expressly disclose that P type can be chosen for the lightly doped wells or body regions (47) from the only two possible doping types. Litwin is cited by the examiner to show that it is indeed art-known that a lightly doped well or body regions in an individual transistor-like varactor can be commonly and desirably doped as P-type when the

source/drain regions being N-type doped in order to form a depletion-type channel region with desirably good channel modulation sensitivity, regardless the individual transistor-like varactor is formed on an SOI type substrate as the one in Chiang or on a bulk-type substrate as the one in Litwin, since the one of the ordinary skill in the art would readily recognize that it is mainly the channel modulation sensitivity that is directly responsible for the main attractive characteristic of a transistor-like varactor—its highly variable capacitance, and such channel modulation takes place only in a very thin carrier-depletable channel-forming region in both of the two types of substrates. And, in either case, well or body region being lightly doped is a necessity for the realization of a carrier-deletable channel-forming region. It further explains why both Chiang and Litwin consistently want the well or body region to be kept lightly doped. Hence, nothing in either Chiang or Litwin is found to be against the combination of the teachings of the two.

Regarding the alleged fourth problem (pages 13 through 15 in the Brief): as already explained above (in response to the second and third alleged problems), both Chiang and Litwin expressly and consistently teach to keep the well or body region as a lightly doped region, as it is necessary in order to form a depletable channel-forming region under the gate dielectric layer. And, for increasing the capacitive switching ratio, i.e., equivalently the dynamical range, of the transistor-like varactor, it is always desirable to reduce the gate-ground overlap with respect to the gate length. As shown in Fig. 2, the overlap between the gate (26) and the ground (23 or 24) in Litwin appears to

be already kept at a substantially minimum, which is in full agreement with what is taught in Equations 11 and/or 14 in Chiang. Therefore, Appellant's arguments about alleged incompatible teachings between Litwin and Chiang is not found convincing.

In addition, it is noted that such arguments about the alleged incompatible teachings is not particularly relevant to the claimed invention, especially to the ones as defined in claims 32-37, in which none of the alleged subject matters about the features of the gate dimension(s), the gate-ground ratio and/or the capacitive switching ratio is directly or indirectly recited. With respect to these features upon which appellant's arguments rely are not recited in the rejected claim(s), it is noted that, although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Regarding the arguments about claims 34 and 35 (pages 15 and 16 in the Brief): as explained in the final rejection, it is art-known that silicon-insulator substrates of both the silicon-on-oxide type (SOI type, which normally naturally includes a highly resistive silicon bottom layer) and the silicon-on-sapphire type (SOS) had become readily available for either N-channel or P-channel type MOS devices, as readily evidenced in the prior art such as Tsang (US 5,563,438; see col. 3, lines 36-37). These substrates each are generally called as a silicon-on-insulator (SOI) substrate as they each have an insulating layer underlying an active top silicon layer for the purpose of increasing device speed and reducing signal loss in the substrate. Each of them has its own art-

recognized advantages and disadvantages over the others in performance and cost. And, it is therefore regarded as to be obvious to the ordinary skill in the art to replace one well-known SOI-type substrate with another well-known SOI-type substrate, as they each provide predictable and well-known results for the resulting devices.

Regarding the arguments about claim 36 (page 17 in the Brief): as pointed in the final rejection, with the p-type lightly doped wells or body regions being formed in the above collectively taught method, N+/P- junctions would be naturally formed therein, which in turn would cause the P-type wells or body regions to be inherently floated electrically, due to the electrical isolation naturally provided by the N+/P- junctions, given that there is no body contact to the light doped wells or body regions in the collectively taught varactor. And, appellant's arguments lack an adequate explanation as to why such electrically floating status would not be inherently established.

Regarding the arguments about claim 39 and 40 (pages 17-18 in the Brief): a varactor with a capacitive switching range as high as or higher than 20 is always commonly desirable to the ordinary skill in the art, in order to achieve a broader controllable capacitance range for it. Various variables including gate width, gate length, and gate-ground overlap are art-recognized result-effective importance parameters for the capacitive switching ratio, and they all are subject to routine experimentation and optimization. It is deemed to be obvious to obtain such high capacitive switching range for the above collectively taught varactor through routine experimentation and

optimization on the art-recognized result-effective parameters, as it has been held that: "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Response to Arguments of ISSUE 2 (Page 19 in the Brief)

The objection to claim 40 set forth in the final rejection has hereby been withdrawn by the examiner after reconsideration.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

SHOUXIANG HU
PRIMARY EXAMINER

Shouxiang Hu
December 22, 2005

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